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EXPOSED LEAD INTERPOSER FRAME PACKAGE

INVENTOR

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] (Not Applicable)

STATEMENT RE: FEDERALLY SPONSORED RESEARCH/DEVELOPMENT

[0002] (Not Applicable)

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0003] The present invention relates to the field of semiconductor packaging. In particular, the present invention relates to a separate interposer structure which may be utilized in a semiconductor package to increase the total input/output capabilities of the semiconductor package.

2. Background Information

[0004] As a result of continuing improvements in semiconductor technology, the specified number of input/output (I/O) leads required to be connected to silicon dies continues to increase. Current designs of standard external lead packages, such as a quad flat package (QFP), thin quad flat package (TQFP) or thin small outline package (TSOP) are not well suited or easily adaptable for the increased number of I/O leads that current state of the art dies require. Furthermore, external lead packages are still utilized in many electronic devices and many manufacturers do not desire to completely redesign their

current motherboard layouts to accommodate semiconductor packages having increased I/O specifications. Moreover, die I/O requirements are even out pacing many of the current land pattern package I/O capabilities, such as micro leadframe packages currently utilized by many electronic manufacturers.

[0005] It would be desirable to provide a device which allows a standard external lead package or a land pattern package to be retrofitted with additional exposed leads or pads/lands to accommodate modern dies having a greater number of I/O's than the original number of I/O's of which the standard external lead package or land pattern package was originally designed to accommodate.

[0006] It would also be desirable to provide a semiconductor package which maintains the current QFP, TQFP, TSOP, or micro leadframe design specifications, yet, is still able to accommodate increased I/O specifications that modern dies require.

BRIEF SUMMARY OF THE INVENTION

[0007] The aforementioned disadvantages are overcome by providing a separate interposer structure which may be integrated into a semiconductor package. Furthermore, the present invention provides a semiconductor package which integrates a separate interposer with an external lead semiconductor package or land pattern semiconductor package to increase the total input/output capabilities of the semiconductor package.

[0008] The interposer constructed in accordance with the present invention is adapted to be integrated into either external lead semiconductor packages such as a quad flat package (QFP), thin quad flat package (TQFP), or thin small outline package (TSOP). In addition to external lead packages, the interposer of the present invention may be integrated into a land pattern semiconductor package such as a micro lead frame package. When integrated into either an external lead semiconductor package or a land pattern semiconductor package, the interposer provides such package with independent exposed lands which supplement the external leads normally provided with an external lead semiconductor package and the exposed pads normally provided with a land pattern semiconductor package. The added lands provide greater design flexibility, and the

capability of standardizing the package footprint without constraints on the size of the semiconductor die of the package.

[0009] The interposer of the present invention also provides the advantages of allowing standard external lead semiconductor packages and land patterns semiconductor packages to be retrofitted with the interposer to allow for the use in the package of a die having an increased number of I/O's. The ability to accommodate the increased I/O semiconductor die is facilitated by the additional lands defined by the interposer. The interposer of the present invention also cost effectively adds additional I/O paths to semiconductor packages, and creates high frequency electrical signal I/O paths on the bottom of the package body of the semiconductor package without degrading the electrical performance thereof. Furthermore, the interposer of the present invention will allow QFP's to have operational frequencies beyond five GHz in a cost effective matter. The interposer of the present invention also provides a cost effective alternative to exposed lead semiconductor packages wherein additional I/O paths are provided as a result of the implementation of a partial saw process. In this regard, by utilizing the interposer, such partial saw process may be eliminated since the interposer may be fabricated separately from the lead frame of the external lead or land pattern semiconductor package.

[0010] The present invention is best understood by reference to the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] These, as well as other features of the present invention, will become more apparent upon reference to the drawings wherein:

[0012] Figure 1A is a top view of a first exemplary embodiment of an interposer structure constructed in accordance with the present invention, referred to as a "½ etch molded" interposer;

[0013] Figure 1B is a cross-section of Figure 1A taken along Section A-A;

[0014] Figure 1C is a cross-section of a second exemplary embodiment of an interposer structure constructed in accordance with the present invention, referred to as a "½ etch molded pedestal" interposer;

[0015] Figures 1D is a top view of a third exemplary embodiment of an interposer structure constructed in accordance with the present invention, referred to as a "downset molded" interposer;

[0016] Figure 1E is a cross-section of Figure 1D taken along Section A-A;

[0017] Figure 1F is a cross-section of a fourth exemplary embodiment of an interposer structure constructed in accordance with the present invention, referred to as a "downset molded pedestal" interposer;

[0018] Figure 2A is a top view of a fifth exemplary embodiment of an interposer structure constructed in accordance with the present invention, referred to as a "½ etch with tape" interposer;

[0019] Figure 2B is a cross-section of Figure 2A taken along Section A-A;

[0020] Figure 2C is a top view of a six exemplary embodiment of an interposer structure constructed in accordance with the present invention, referred to as a "downset with tape" interposer;

[0021] Figure 2D is a cross-section of Figure 2C taken along Section A-A;

[0022] Figure 3A is an illustrative cross-sectional view of a seventh exemplary embodiment of the present invention in which an external lead semiconductor package is provided with the "½ etch molded pedestal" interposer structure;

[0023] Figure 3B is an illustrative cross-sectional view of an eighth exemplary embodiment of the present invention in which an external lead semiconductor package is provided with the "½ etch molded" interposer structure;

[0024] Figure 4A is an illustrative cross-sectional view of a ninth exemplary embodiment of the present invention in which an external lead semiconductor package is provided with the "downset molded pedestal" interposer structure;

[0025] Figure 4B is an illustrative cross-sectional view of a tenth exemplary embodiment of the present invention in which an external lead semiconductor package is provided with the "downset molded" interposer structure;

[0026] Figure 5A is an illustrative cross-sectional view of a eleventh exemplary embodiment of the present invention in which an external lead semiconductor package is provided with the "½ etch with tape" interposer structure;

[0027] Figure 5B is an illustrative cross-sectional view of a twelfth exemplary embodiment of the present invention in which an external lead semiconductor package is provided with the "downset with tape" interposer structure;

[0028] Figure 6A is an illustrative cross-sectional view of a thirteenth exemplary embodiment of the present invention in which a land pattern semiconductor package is provided with the "½ etch molded pedestal" interposer structure;

[0029] Figure 6B is an illustrative cross-sectional view of a fourteenth exemplary embodiment of the present invention in which a land pattern semiconductor package is provided with the "½ etch molded" interposer structure;

[0030] Figure 7A is an illustrative cross-sectional view of a fifteenth exemplary embodiment of the present invention in which a land pattern semiconductor package is provided with the "downset molded pedestal" interposer structure;

[0031] Figure 7B is an illustrative cross-sectional view of a sixteenth exemplary embodiment of the present invention in which a land pattern semiconductor package is provided with the "downset molded" interposer structure;

[0032] Figure 8A is an illustrative cross-sectional view of a seventeenth exemplary embodiment of the present invention in which a land pattern semiconductor package is provided with the "½ etch with tape" interposer structure;

[0033] Figure 8B is an illustrative cross-sectional view of a eighteenth exemplary embodiment of the present invention in which a land pattern semiconductor package is provided with the "downset with tape" interposer structure;

[0034] Figure 9A is an illustrative cross-sectional view of a nineteenth exemplary embodiment of the present invention in which an external lead semiconductor package is provided with an inverted "½ etch molded pedestal" interposer having a second external lead semiconductor package electrically connected thereto;

[0035] Figure 9B is an illustrative cross-sectional view of a twentieth exemplary embodiment of the present invention in which an external lead semiconductor package is provided with an inverted "½ etch molded" interposer having a second external lead semiconductor package electrically connected thereto;

[0036] Figure 10A is an illustrative cross-sectional view of a twenty-first exemplary embodiment of the present invention in which an external lead semiconductor package is

provided with an inverted "downset molded pedestal" interposer having a second external lead semiconductor package electrically connected thereto;

[0037] Figure 10B is an illustrative cross-sectional view of a twenty-second exemplary embodiment of the present invention in which an external lead semiconductor package is provided with an inverted "downset molded" interposer having a second external lead semiconductor package electrically connected thereto;

[0038] Figure 11A is an illustrative cross-sectional view of a twenty-third exemplary embodiment of the present invention in which an external lead semiconductor package is provided with an inverted "½ etch with tape" interposer having a second external lead semiconductor package electrically connected thereto;

[0039] Figure 11B is an illustrative cross-sectional view of a twenty-fourth exemplary embodiment of the present invention in which an external lead semiconductor package is provided with an inverted "downset with tape" interposer having a second external lead semiconductor package electrically connected thereto;

[0040] Figure 12A is an illustrative cross-sectional view of a twenty-fifth exemplary embodiment of the present invention in which a land pattern semiconductor package with the "½ etch molded pedestal" interposer has a second external lead semiconductor package electrically connected thereto;

[0041] Figure 12B is an illustrative cross-sectional view of a twenty-sixth exemplary embodiment of the present invention in which a land pattern semiconductor package with the "½ etch molded" interposer has a second external lead semiconductor package electrically connected thereto;

[0042] Figure 13A is an illustrative cross-sectional view of a twenty-seventh exemplary embodiment of the present invention in which a land pattern semiconductor package with the "downset molded pedestal" interposer has a second external lead semiconductor package electrically connected thereto;

[0043] Figure 13B is an illustrative cross-sectional view of a twenty-eighth exemplary embodiment of the present invention in which a land pattern semiconductor package with the "downset molded" interposer has a second external lead semiconductor package electrically connected thereto;

[0044] Figure 14A is an illustrative cross-sectional view of a twenty-ninth exemplary embodiment of the present invention in which a land pattern semiconductor package with the "½ etch with tape" interposer has a second external lead semiconductor package electrically connected thereto; and

[0045] Figure 14B is an illustrative cross-sectional view of a thirtieth exemplary embodiment of the present invention in which a land pattern semiconductor package with the "downset with tape" interposer has a second external lead semiconductor package electrically connected thereto.

[0046] Common reference numeral are used throughout the drawings and detailed description to indicate like elements.

DETAILED DESCRIPTION OF THE INVENTION

[0047] The particulars shown herein are by way of example and for purposes of illustrative discussion of the embodiments of the present invention only and are presented in the cause of providing what is believed to the most useful and readily understood description of the principles and conceptual aspects of the present invention. In this regard, no attempt is made to show structural details of the present invention in more detail than is necessary for the fundamental understanding of the present invention, the description taken with the drawings making apparent to those skilled in the art how the several forms of the present invention may be embodied in practice.

Overview of Separate Interposer Structure Embodiments

[0048] Figures 1A-F and 2A-D illustrate numerous embodiments of a separately constructed interposer according to an aspect of the present invention. Six basic embodiments of a separate interposer (reference numerals 1, 2, 3, 4, 5 or 6) are presented for exemplary purposes, including: "½ etch molded" interposer 1 (Figure 1A); "½ etch molded pedestal" interposer 2 (Figure 1C); "downset molded" interposer 3 (Figure 1D); "downset molded pedestal" interposer 4 (Figure 1F); "½ etch with tape" interposer 5 (Figure 2A); and "downset with tape" interposer 6 (Figure 2B). The interposer may also take the form of numerous other embodiments having a variety of permutations and combinations of the features discussed within the specification, and therefore, the

interposer of the present invention should not be limited only to the illustrated embodiments.

½-Etch Molded Embodiments

[0049] Figure 1A depicts a first exemplary embodiment of an interposer structure, referred to as the "½ etch molded" interposer 1, according to an aspect of the present invention, and Figure 1B is a cross-section of the same taken along Section A-A.

[0050] The "½ etch molded" interposer 1 has a thin rectangular or square shape, and is composed of three primary components: die pad 18, a plurality of interposer leads 16, and a molded dielectric 14. Interposer 1 is formed by embedding die pad 18 and the plurality of interposer leads 16 into a molded dielectric 14 which defines the body of the interposer 1. Dielectric 14 may be a typical transfer molded epoxy mold compound, or a high melting point thermoplastic such as a Liquid Crystal Polymer (LCP). As a result, die pad 18 and each of the interposer leads 16 are independently insulated from each other by the molded dielectric 14. Additionally, interposer 1 includes a cavity 40 defined by vertically oriented perimeter walls formed within a central upper region of dielectric 14. Cavity 40 exposes a portion of the top surface of the die pad 18 to allow for the attachment of a silicon die 32 thereto.

[0051] Die pad 18 has a thin, flat rectangular or square shape and is constructed from an electrically conductive material such as Cu alloy. Die pad 18 is configured and oriented such that it defines a portion of the lower surface of the interposer 1. The side edges and peripheral portions of the top surface of die pad 18 are encased or covered by dielectric 14. The entire bottom surface of die pad 18 is exposed in the dielectric 14. The totally exposed bottom surface of die pad 18 is larger in size than conventional standard die pads, and therefore, allows for greater thermal dissipation and better thermal performance.

[0052] Interposer leads 16 may be made from an electrically conductive material such as Cu alloy and are designed to create a high-speed microstrip structure for controlling impedance in which die pad 18 acts as a ground reference voltage. As shown in Figures 1B and 1C, each interposer lead 16 has an elongate finger portion 46 which defines an exterior terminal end 48 and an interior terminal end 49. Projecting

downwardly from the finger portion 46 is a protuberance 47, the distal end of which defines a land 50. The land 50 of each lead 16 may be utilized as a solder connection terminal for soldering interposer 1 (when integrated into a semiconductor package as discussed below) to an underlying substrate such as a circuit board 28 (as shown in Figure 3A). The top surface of the finger portion 46 adjacent the interior terminal end 49 (which terminates at the perimeter wall of the cavity 40) is adapted to receive one end of a wire bond 54 (e.g., Au wire bond), the opposite end of which extends to the die 32. The finger portions 46 of the leads 16 are arranged on the dielectric 14 in four sets, the leads 16 of each set being separated by the dielectric 14 for electrical insulation.

[0053] As is shown in Figures 1A-C, though the interposer leads 16 are substantially embedded within the top surface of the molded dielectric 14, the top surfaces of the finger portions 46 of the leads 16 are exposed. In each of the four sets of leads 16 included with the interposer 1, the interior terminal end 49 of the finger portion 46 of each lead 16 extends to and partially defines one of the vertically oriented perimeter walls of the cavity 40. The finger portions 46 are further arranged such that they initially spread outward in a fan-like pattern toward the outer peripheral edge of the dielectric 14. The exterior terminal ends 49 of the fingers 46 extend beyond the outer peripheral edge of the dielectric 14, as do the downwardly projecting protuberances 47 which, as indicated above, define the lands 50. From the perspective of Figure 1A (a top plan view of the interposer 1), it is shown that the width of each lead 16 is initially thin and tapered at the interior terminal end 49 of the finger portion 46, and progressively widens to the exterior terminal end 48, those sections of the finger portions 46 defining the exterior terminal ends 48 extending in spaced, generally parallel relation to each other to a point beyond the outer peripheral edge of the dielectric 14.

[0054] Figure 1C provides a cross-section of a second exemplary embodiment of an interposer structure, referred to as a "½ etch molded pedestal" interposer 2, according to an aspect of the present invention. The difference between interposer 1 and interposer 2 is the inclusion of a molded pedestal 20 in interposer 2. A function of molded pedestal 20 is to provide support for package leads 34 (see Figure 3A) when interposer 2 is being integrated into a semiconductor package 8.

[0055] Molded pedestal 20 extends above the finger portions 46 of interposer leads 16 and is integrally formed with molded dielectric 14. Pedestal 20 has an inner perimeter wall and an outer perimeter wall which are interconnected by an upper surface of pedestal 20 which is substantially flat and parallel to both the top surfaces of the interposer leads 16 and the top surface of die pad 18. The inner perimeter pedestal wall is spaced outward from the perimeter walls of cavity 40 such that a portion of the top surface of the finger portion 46 of each of the interposer leads 16 is still exposed between cavity 40 and the inner perimeter pedestal wall. Also, the outer perimeter wall of the pedestal 20 is spaced inward from the outer peripheral edge of the dielectric 14 such that distal portion of the top surface of the finger portion 46 of each of the interposer leads 16 is still exposed. However, the pedestal 20 may extend to the outer peripheral edge of the dielectric 14 such that only that portion of the top surface of each finger portion 46 between the cavity 40 and the inner perimeter pedestal wall is exposed.

Downset Molded Embodiments

[0056] Figure 1D illustrates a top view of a third exemplary embodiment of an interposer structure, referred to as a "downset molded" interposer 3, according to an aspect of the present invention, and Figure 1E is a cross-section taken of the same along Section A-A.

[0057] The interposer 3 has features similar to those of the interposers 1, 2 above, except for the specific design of the interposer leads 16 used in interposer 3. In the third embodiment, interposer leads 16 each have a downset 38 which defines a land 50 (or exposed lead). In the "downset molded" interposer 3, the lands 50 are positioned closer toward the peripheral edge of die pad 18, as compared to the lands 50 in the interposers 1, 2. In particular, the downset 38 begins at about a thirty to forty-five degree angle downward just above the peripheral edge of die pad 18, and then straightens out so that the land 50 is generally co-planar with the bottom surface of the die pad 18. The downset 38 then returns upward at about a thirty to forty-five degree angle until it reaches the exterior terminal end 48 of the corresponding interposer lead 16. Land 50 provides an exposed lead or pad on the lower surface of the interposer 3 which may be utilized as a solder connection terminal for soldering interposer 3 to circuit board 28.

[0058] Figure 1F illustrates a cross-section of a fourth exemplary embodiment of an interposer structure, referred to as a "downset molded pedestal" interposer 4, according to an aspect of the present invention. The difference between the third and fourth embodiments is that the "downset molded pedestal" interposer 4 includes a molded pedestal 20 which extends above the top surfaces of the finger portions 46 of interposer leads 16. The molded pedestal 20 is similar to the molded pedestal 20 previously described with respect to the second embodiment ("½ etch molded pedestal interposer 2"), and therefore, the specific details are not described again.

½-Etch With Tape Embodiments

[0059] Figure 2A illustrates a top view of a fifth exemplary embodiment of an interposer structure, referred to as a "½ etch with tape" interposer 5, according to an aspect of the present invention, and Figure 2B is a cross-section of the same taken along Section A-A.

[0060] In the fifth embodiment, die pad 18 and the interposer leads 16 are the same as those described in the previous embodiments; however, the "½ etch with tape" interposer 5 does not include the molded dielectric 14. Instead, interposer 5 utilizes a nonconductive adhesive tape 22 or similar material that acts as a structural member to connect the undersides of finger portions 46 of the interposer leads 16 to a peripheral portion of the top surface of die pad 18. This embodiment is ideally suited for less complex exposed lead structures that are less prone to damage or stability problems.

[0061] In particular, adhesive tape 22 is applied to the top surface of die pad 18 along the square or rectangular outer peripheral edge of die pad 18. A portion of die pad 18 is left uncovered to receive die 32. The interposer leads 16 are shaped and arranged in a similar manner as those described in the first embodiment (see "½ etch molded interposer 1"). However, in the interposer 5 the lower surfaces of the finger portions 46 of each set are affixed to the top surface of the adhesive tape 22 such that the interior terminal ends 49 of the interposer leads 16 are flush with the perimeter wall of cavity 40 defined by the adhesive tape 22. The finger portions 46 are affixed to adhesive tape 22 so as to extend in generally parallel relation to the die pad 18.

Downset With Tape Embodiments

[0062] Figure 2C illustrates a top view of a six exemplary embodiment of an interposer structure, referred to as a "downset with tape" interposer 6, according to an aspect of the present invention, and Figure 2D is a cross-section of the same taken along Section A-A.

[0063] The interposer 6 is very similar to the "½ etched with tape" interposer 5 above, however, interposers leads 16 have a downset 38 as in the interposers 3, 4 which provides a land 50 that functions as an exposed pad as will be described below. Thus, in the interposer 6, lands 50 are positioned closer toward the peripheral edge of the die pad 18, as compared to the lands 50 in interposers 1, 2 and 5. In particular, the downset 38 begins at about a thirty to forty-five degree angle downward just above the outer peripheral edge of die pad 18 and then straightens out so that the land 50 is generally co-planar to the bottom surface of the die pad 18. The downset 38 then returns upward at about a thirty to forty-five degree angle until it reaches the exterior terminal end 48 of interposer lead 16.

Embodiments of Interposers Integrated into Standard External Lead Packages

[0064] Figures 3A-B through and 5A-B illustrate various embodiments of the present invention that are semiconductor packages which include one of the interposer structures 1-6 integrated into an external lead semiconductor package such as a quad flat package (QFP), thin quad flat package (TQFP) or thin small outline package (TSOP). It is noted that interposers 1-6 may be integrated into a variety of standard external lead packages, and therefore, the present invention should not be limited only to the exemplary embodiments described below.

[0065] Figure 3A is a cross-sectional view of a seventh exemplary embodiment of the present invention depicting an external lead semiconductor package 10A which is assembled to include the "½ etch molded pedestal" interposer 2 described above. In the semiconductor package 10A, the interposer 2 has the structural attributes described above in relation to Figure 1C. In fabricating the semiconductor package 10A, the leadframe of

the semiconductor package 10A is interfaced to the interposer 2 in a manner wherein the inner portions of the leads 34 of the leadframe are rested upon the top surface of the pedestal 20 of the interposer 2. It is contemplated that the leads 34 of the leadframe may be adhered (e.g., glued) directly to the top surface of the pedestal 20, or secured thereto via a welding or riveting procedure. Thereafter, the semiconductor die 32 is placed within the cavity 40 of the interposer 2, and attached to the exposed portion of the top surface of the die pad 18. The attachment procedure is in accordance with standard assembly processes wherein a conductive epoxy adhesive is used to attach the die 32 directly to the top surface of the die pad 18.

[0066] Thereafter, the terminals of the semiconductor die 32 are electrically connected to the interposer leads 16 and, in particular, to the top surfaces of the finger portions 46 which extend to the interior terminal ends 49 and are not covered by the pedestal 20. Such electrical connection is facilitated through the use of wire bonds 54. The wire bonds 54 are also used to electrically connect the terminals of the die 32 to the inner portions of the leads 34, and may also be optionally used to electrically connect the die 32 directly to the die pad 18 of the interposer 2. A conventional bonding process, such as Au thermosonic wire bonding methods, may be employed in the fabrication of the external lead semiconductor package 10A. Those of ordinary skill in the art will recognize that the wire bonds 54 may be electrically connected to the interposer leads 16, leads 34, and/or die pad 18 in any number or in any combination without departing from the spirit and scope of the present invention. Once the semiconductor die 32 has been electrically connected to the interposer 2 and leadframe engaged thereto, the interposer 2, die 32, and leadframe are partially covered or encapsulated by a plastic compound which, upon hardening, forms a package body 36 of the semiconductor package 10A. As seen in Figure 3A, the package body 36 is formed in a manner wherein the lands 50 defined by the interposer leads 16 of the interposer 2 and the bottom surface of the die pad 18 of the interposer 2 are each exposed in and substantially flush with the bottom surface defined by the package body 36. The leads 34 of the leadframe of the semiconductor package 10A protrude from respective side surfaces of the package body 36. Also exposed within the bottom surface of the package body 36 is a portion of the dielectric 14 of the

interposer 2. The die 32 and wire bonds 54 are completely covered or encapsulated by the package body 36.

[0067] Subsequent to the formation of the package body 36, the dambar of the leadframe which is disposed outboard of the package body 36 and interconnects the leads 34 to each other is singulated or removed from the leads 34, thus effectively electrically isolating the leads 34 from each other. Thereafter, the leads 34 may be subjected to a bending operation to impart the gull-wing configuration thereto as shown in Figure 3A.

[0068] The completed semiconductor package 10A, by virtue of the inclusion of the interposer 2 therein, includes not only the terminals defined by the exposed leads 34, but also those defined by the exposed lands 50 of the interposer leads 16 of the interposer 2. Another terminal is defined by the exposed bottom surface of the die pad 18. As seen in Figure 10A, the distal ends of the leads 34, lands 50, and die pad 18 may each be connected to an underlying substrate such as the printed circuit board 28 for purposes of providing signal routing or, in the case of the die pad 18, a ground connection or medium for enhanced thermal dissipation.

[0069] Figure 3B is a cross-sectional view of an eighth exemplary embodiment of the present invention in which an exposed lead semiconductor package 10B is provided with the "½ etch molded" interposer 1 shown and described in relation to Figures 1A and 1B. In the semiconductor package 10B, adhesive tape 23 is substituted for the pedestal 20 of the interposer 2. In this regard, the fabrication process associated with the semiconductor package 10B of the eighth embodiment is substantially identical to that described above in relation to the semiconductor package 10A, except that the inner portions of the leads 34 of the leadframe in the semiconductor package 10B are adhered to the adhesive tape 23, as opposed to being interfaced to the pedestal 20 of the interposer 2 as described in relation to Figure 10A. In fabricating the semiconductor package 10B, the adhesive tape 23 should be sufficiently thick to ensure a low coupling capacitance between the leads 34 of the leadframe and the interposer leads 16 of the interposer 1.

[0070] Figures 4A, 4B, 5A and 5B illustrate external lead semiconductor packages 10C, 10D, 10E and 10F, respectively, constructed in accordance with ninth through twelfth exemplary embodiments of the present invention. Because the semiconductor packages 10C, 10D, 10E and 10F are fabricated through an assembly process

substantially similar to that described above in relation to the semiconductor packages 10A, 10B, only an overview of the overall configuration of the ninth through twelfth embodiments is discussed below.

[0071] Figure 4A is a cross-sectional view of the ninth exemplary embodiment of the present invention in which the external lead semiconductor package 10C is provided with the "downset molded pedestal" interposer 4 as an alternative to the "½ etch molded pedestal" interposer 2 shown and described in relation to Figure 3A. In the semiconductor package 10C, the lands 50 defined by the downsets 38 of the interposer leads 16 of the interposer 4 are exposed in and substantially flush with the bottom surface of the package body 36. Also exposed in the bottom surface of the package body 36 is the bottom surface of the die pad 18 of the interposer 4, as well as portions of the dielectric 14 thereof.

[0072] Figure 4B is a cross-sectional view of the tenth exemplary embodiment of the present invention in which the semiconductor package 10D is provided with the "downset molded" interposer 3 shown and described in relation to Figures 1D and 1E, as an alternative to the interposer 4 shown in Figure 4A. As in the semiconductor package 10B described above in relation to Figure 3B, the leads 34 of the semiconductor package 10D are interfaced to the interposer 3 through the use of the adhesive tape 23.

[0073] Figure 5A is a cross-sectional view of the eleventh exemplary embodiment of the present invention in which the semiconductor package 10E is fabricated to include the "½ etch with tape" interposer 5 previously shown and described in relation to Figures 2A and 2B. In the semiconductor package 10E, adhesive tape 23 is also used to cooperatively engage the leads 34 of the leadframe included in the semiconductor package 10E to the top surfaces of the finger portions 46 of the interposer leads 16 included in the interposer 5.

[0074] Figure 5B is a cross-sectional view of the twelfth exemplary embodiment of the present invention in which the semiconductor package 10F is assembled to include the "downset with tape" interposer 6 shown and described in relation to Figures 2C and 2D, as an alternative to the "½ etch with tape" interposer 5 included in the semiconductor package 10E as shown in Figure 5A. In the semiconductor package 10F, adhesive tape

23 is also used to cooperatively engage the leads 34 to the top surfaces of the finger portions 46 of the interposer leads 16 included in the interposer 6.

Embodiments of Interposers Integrated into Land Pattern Packages

[0075] Figures 6A-B through 8A-B illustrate various embodiments of the present invention that are semiconductor packages which include one of the interposer structures 1-6 integrated into a land pattern semiconductor package, such as a microleadframe package. It is noted that the interposers 1-6 may be integrated into a variety of land pattern packages, and therefore, the present invention should not be limited only to the exemplary embodiments described below.

[0076] Figure 6A is a cross-sectional view of a thirteenth exemplary embodiment of the present invention depicting a land pattern semiconductor package 11A which is assembled to include the "½ etch molded pedestal" interposer 2 described above. In the semiconductor package 11A, the interposer 2 has the structural attributes described above in relation to Figure 1C. The process of fabricating the semiconductor package 11A is substantially similar to that described above in relation to the fabrication of the semiconductor package 10A shown in Figure 3A. In this regard, the primary distinction between the semiconductor packages 10A, 11A lies in the configuration of the package body 36 of the semiconductor package 11A in comparison to the package body 36 of the semiconductor package 10A. More particularly, in the semiconductor package 11A, the leads 34 of the leadframe thereof are also cooperatively engaged to the top surface of the pedestal 20 of the interposer 2. The package body 36 of the semiconductor package 11A is formed such that the bottom surfaces of the distal portions of the leads 34 of the leadframe are exposed in and substantially flush with the bottom surface of the package body 36. This is in contrast to the relationship between the leads 34 and the package body 36 in the semiconductor package 10A wherein the outer portions of the leads 34 protrude from respective side surfaces of the package body 36 in the semiconductor package 10A. The absence of any portion of the leads 34 protruding from the package body 36 in the semiconductor package 11A imparts thereto the structural attributes of a land pattern semiconductor package. Once the package body 36 of the semiconductor package 11A has been completely formed, any portion of the leadframe protruding from

the package body 36 is singulated or removed, thus resulting in the bottom surfaces of the distal portions of the leads 34 being exposed in and substantially flush with the bottom surface of the package body 36, and the distal end of each lead 34 being exposed in and substantially flush with a respective side surface of the package body 36.

[0077] Figure 11B is a cross-sectional view of a fourteenth exemplary embodiment of the present invention in which a land pattern semiconductor package 11B is provided with the "½ etch molded" interposer 1 shown and described in relation to Figures 1A and 1B. In the semiconductor package 11B, adhesive tape 23 is substituted for the pedestal 20 of the interposer 2 shown in Figure 11A. In this regard, the fabrication process associated with the semiconductor package 11B of the fourteenth embodiment is substantially identical to that described above in relation to the semiconductor package 11A, except that the inner portions of the leads 34 of the leadframe in the semiconductor package 11B are adhered to the adhesive tape 23, as opposed to being interfaced to the pedestal 20 of the interposer 2 as described in relation to Figure 11A.

[0078] Figures 7A, 7B, 8A and 8B illustrate land pattern semiconductor packages 11C, 11D, 11E and 11F, respectively, constructed in accordance with fifteenth through eighteenth embodiments of the present invention. Because the semiconductor packages 11C, 11D, 11E and 11F are fabricated through an assembly process substantially similar to that described above in relation to the semiconductor packages 11A, 11B, only an overview of the overall configuration of the fifteenth through eighteenth embodiments is discussed below.

[0079] Figure 7A is a cross-sectional view of the fifteenth exemplary embodiment of the present invention in which the land pattern semiconductor package 11C is provided with the "downset molded pedestal" interposer 4 as an alternative to the "½ etch molded pedestal" interposer 2 shown and described in relation to Figure 11A. In the semiconductor package 11C, the lands 50 defined by the downsets 38 of the interposer leads 16 of the interposer 4 are exposed in and substantially flush with the bottom surface of the package body 36. Also exposed in the bottom surface of the package body 36 is the bottom surface of the die pad 18 of the interposer 4, as well as portions of the dielectric 14 thereof.

[0080] Figure 7B is a cross-sectional view of the sixteenth exemplary embodiment of the present invention in which the land pattern semiconductor package 11D is provided with the "downset molded" interposer 3 shown and described in relation to Figures 1D and 1E, as an alternative to the interposer 4 shown in Figure 7A. As in the semiconductor package 11B described above in relation to Figure 6B, the leads 34 of the semiconductor package 11D are interfaced to the interposer 3 through the use of the adhesive tape 23.

[0081] Figure 8A is a cross-sectional view of the seventeenth exemplary embodiment of the present invention in which the land pattern semiconductor package 11E is fabricated to include the "½ etch with tape" interposer 5 previously shown and described in relation to Figures 2A and 2B. In the semiconductor package 11E, adhesive tape 23 is also used to cooperatively engage the leads 34 of the leadframe included in the semiconductor package 11E to the top surfaces of the finger portions 46 of the interposer leads 16 included in the interposer 5.

[0082] Figure 8B is a cross-sectional view of the eighteenth exemplary embodiment of the present invention in which the land pattern semiconductor package 11F is assembled to include the "downset with tape" interposer 6 shown and described in relation to Figures 2C and 2D, as an alternative to the "½ etch with tape" interposer 5 included in the semiconductor package 11E as shown in Figure 8A. In the semiconductor package 11F, adhesive tape 23 is also used to cooperatively engage the leads 34 to the top surfaces of the finger portions 46 of the interposer leads 16 included in the interposer 6.

Embodiments of Stacked External Lead Packages Including Interposers

[0083] Figures 9A-B through 11A-B illustrate various embodiments of the present invention wherein external lead semiconductor packages assembled to include the interposers 1-6 described above have a second, standard external lead semiconductor package stacked thereon and electrically connected thereto. As will be discussed in more detail below, in each of the embodiments of the "stacked" external lead semiconductor packages, the interposers 1-6 are inverted as compared to the showings in prior embodiments.

[0084] Figure 9A is a cross-sectional view of a nineteenth exemplary embodiment of the present invention comprising a stacked semiconductor package arrangement including an external lead semiconductor package 10A' which bears close similarity to the structural and functional attributes of the semiconductor package 10A shown in Figure 3A. The semiconductor package 10A' includes the interposer 2 described above. However, in contrast to the orientation of the interposer 2 in the semiconductor package 10A, the interposer 2 in the semiconductor package 10A' is inverted such that the top surfaces of the leads 34 of the leadframe in the semiconductor package 10A' are placed against the pedestal 20 of the interposer 2 thereof. This is in contrast to the semiconductor package 10A described above wherein the bottom surfaces or undersides of the leads 34 thereof are rested against the pedestal 20 of the corresponding interposer 2. Due to the interposer 2 in the semiconductor package 10A' being inverted, the lands 50 and bottom surface of the die pad 18 of the interposer 2 in the semiconductor package 10A' are exposed in the top surface (rather than the bottom surface) of the package body 36 thereof. As a result, when the leads 34 of the semiconductor package 10A' are attached to an underlying substrate such as a printed circuit board 28, the exposed lands 50 in the top surface of the package body 36 provide connection terminals which allow for the electrical connection of a second external lead semiconductor package 58 to the semiconductor package 10A' in the manner shown in Figure 9A. In this regard, the distal ends of the leads of the second, uppermost semiconductor package 58 are brought into contact with and electrically connected to respective ones of the lands 50 of the interposer 2 of the semiconductor package 10A', the lands 50 being exposed in and substantially flush with the top surface of the package body 36 of the semiconductor package 10A' as indicated above.

[0085] Figure 9B is a cross-sectional view of a twentieth exemplary embodiment of the present invention which shows a stacked semiconductor package arrangement similar to that shown in Figure 9A, except that the semiconductor package 10A' shown in Figure 9A is substituted with the semiconductor package 10B' shown in Figure 9B, the semiconductor package 10B' including the above-described interposer 1 as an alternative to the interposer 2 included in the semiconductor package 10A'. In this regard, the semiconductor package 10B' itself bears substantial similarity to the semiconductor

package 10B shown and described above in relation to Figure 3B, except that the interposer 1 in the semiconductor package 10B' is inverted in the same manner the interposer 2 is inverted in the semiconductor package 10A'. The inversion of the interposer 1 in the semiconductor package 10B' facilitates the exposure of the lands 50 of the interposer 1 in the top surface of the package body 36 of the semiconductor package 10B', thus allowing for the electrical connection of the second external lead semiconductor package 58 thereto.

[0086] Figure 10A is a cross-sectional view of a twenty-first exemplary embodiment of the present invention which shows a stacked semiconductor arrangement similar to that shown in Figure 9A except that the semiconductor package 10C' shown in Figure 10A includes the above-described interposer 4 as an alternative to the interposer 2 included in the semiconductor package 10A'. In this regard, the semiconductor package 10C' bears substantial similarity to the semiconductor package 10C shown in Figure 4A, except that the interposer 4 in the semiconductor package 10C' is inverted in the same manner the interposer 2 is inverted in the semiconductor package 10A'. The inversion of the interposer 4 in the semiconductor package 10C' facilitates the exposure of the lands 50 of the interposer 4 in the top surface of the package body 36 of the semiconductor package 10C', thus allowing for the electrical connection of the second external lead semiconductor package 58 thereto.

Figure 10B is a cross-sectional view of a twenty-second exemplary embodiment of the present invention which shows a stacked semiconductor arrangement also similar to that shown in Figure 9A, except that the semiconductor package 10D' shown in Figure 10B includes the above-described interposer 3 as an alternative to the interposer 2 included in the semiconductor package 10A'. In this regard, the semiconductor package 10D' itself bears substantial similarity to the semiconductor package 10D shown and described above in relation to Figure 4B, except that the interposer 3 in the semiconductor package 10D' is inverted in the same manner the interposer 2 is inverted in the semiconductor package 10A'. The inversion of the interposer 3 in the semiconductor package 10D' facilitates the exposure of the lands 50 of the interposer 3 in the top surface of the package body 36 of the semiconductor package

10D', thus allowing for the electrical connection of the second external lead semiconductor package 58 thereto.

Figure 11A is a cross-sectional view of a twenty-third exemplary embodiment of the present invention which shows a stacked semiconductor arrangement also similar to that shown in Figure 9A, except that the semiconductor package 10E' shown in Figure 11A includes the above-described interposer 5 as an alternative to the interposer 2 included in the semiconductor package 10A'. In this regard, the semiconductor package 10E' itself bears substantial similarity to the semiconductor package 10E shown and described above in relation to Figure 5A, except that the interposer 5 in the semiconductor package 10E' is inverted in the same manner the interposer 2 is inverted in the semiconductor package 10A'. The inversion of the interposer 5 in the semiconductor package 10E' facilitates the exposure of the lands 50 of the interposer 5 in the top surface of the package body 36 of the semiconductor package 10E', thus allowing for the electrical connection of the second external lead semiconductor package 58 thereto.

Figure 11B is a cross-sectional view of a twenty-fourth exemplary embodiment of the present invention which shows a stacked semiconductor arrangement similar to that shown in Figure 9A, except that the semiconductor package 10F' shown in Figure 11B includes the above-described interposer 6 as an alternative to the interposer 2 included in the semiconductor package 10A'. In this regard, the semiconductor package 10F' itself bears substantial similarity to the semiconductor package 10F shown and described above in relation to Figure 5B, except that the interposer 6 in the semiconductor package 10F' is inverted in the same manner the interposer 2 is inverted in the semiconductor package 10A'. The inversion of the interposer 6 in the semiconductor package 10F' facilitates the exposure of the lands 50 of the interposer 6 in the top surface of the package body 36 of the semiconductor package 10F', thus allowing for the electrical connection of the second external lead semiconductor package 58 thereto.

Embodiments of Stacked Land Pattern Packages Including Interposers

Figures 12A-B through 14A-B illustrate various embodiments of the present invention wherein land pattern semiconductor packages assembled to include the

interposers 1-6 described above have a second, standard external lead semiconductor package stacked thereon and electrically connected thereto.

Figure 12A is a cross-sectional view of a twenty-fifth exemplary embodiment of the present invention comprising a stacked semiconductor package arrangement including a land pattern semiconductor package 11A' which bears close similarity to the structural and functional attributes of the semiconductor package 11A shown in Figure 6A. The semiconductor package 11A' includes the interposer 2 described above. However, in contrast to the orientation of the leads 34 in the semiconductor package 11A, the leads 34 in the semiconductor package 11A' are inverted such that the top surfaces of the leads 34 of the leadframe in the semiconductor package 11A' are placed against the pedestal 20 of the interposer 2 thereof. This is in contrast to the semiconductor package 11A described above wherein the bottom surfaces or undersides of the leads 34 thereof are rested against the pedestal 20 of the corresponding interposer 2. Due to the leads 34 in the semiconductor package 11A' being inverted, the bottom surfaces of the distal portions thereof are exposed in the top surface (rather than the bottom surface) of the package body 36 of the semiconductor package 11A'. As a result, when the lands 50 of the interposer 2 in the semiconductor package 11A' are attached to an underlying substrate such as a printed circuit board 28, the exposed portions of the bottom surfaces of the leads 34 in the top surface of the package body 36 provide connection terminals which allow for the electrical connection of a second external lead semiconductor package 58 to the semiconductor package 11A' in the manner shown in Figure 12A.

Figure 12B is a cross-sectional view of a twenty-sixth exemplary embodiment of the present invention which shows a stacked semiconductor package arrangement similar to that shown in Figure 12A, except that the semiconductor package 11B' shown in Figure 12B includes the above-described interposer 1 as an alternative to the interposer 2 included in the semiconductor package 11A'. In this regard, the semiconductor package 11B' itself bears substantial similarity to the semiconductor package 11B shown and described above in relation to Figure 6B, except that the leads 34 in the semiconductor package 11B' are inverted in the same manner the leads 34 are inverted in the semiconductor package 11A'. The inversion of the leads 34 in the semiconductor

package 11B' allows for the electrical connection of the second external lead semiconductor package 58 thereto in the manner shown in Figure 12B.

Figure 13A is a cross-sectional view of a twenty-seventh exemplary embodiment of the present invention which shows a stacked semiconductor package arrangement similar to that shown in Figure 12A, except that the semiconductor package 11C' shown in Figure 13A includes the above-described interposer 4 as an alternative to the interposer 2 included in the semiconductor package 11A'. In this regard, the semiconductor package 11C' itself bears substantial similarity to the semiconductor package 11C shown and described above in relation to Figure 7A, except that the leads 34 in the semiconductor package 11C' are inverted in the same manner the leads 34 are inverted in the semiconductor package 11A'. The inversion of the leads 34 in the semiconductor package 11C' allows for the electrical connection of the second external lead semiconductor package 58 thereto in the manner shown in Figure 13A.

Figure 13B is a cross-sectional view of a twenty-eighth exemplary embodiment of the present invention which shows a stacked semiconductor package arrangement similar to that shown in Figure 12A, except that the semiconductor package 11D' shown in Figure 13B includes the above-described interposer 3 as an alternative to the interposer 2 included in the semiconductor package 11A'. In this regard, the semiconductor package 11D' itself bears substantial similarity to the semiconductor package 11D as shown and described above in relation to Figure 11D, except that the leads 34 in the semiconductor package 11D' are inverted in the same manner the leads 34 are inverted in the semiconductor package 11A'. The inversion of the leads 34 in the semiconductor package 11D' allows for the electrical connection of the second external lead semiconductor package 58 thereto in the manner shown in Figure 13B.

Figure 14A is a cross-sectional view of a twenty-ninth exemplary embodiment of the present invention which shows a stacked semiconductor package arrangement similar to that shown in Figure 12A, except that the semiconductor package 11E' shown in Figure 14A includes the above-described interposer 5 as an alternative to the interposer 2 included in the semiconductor package 11A'. In this regard, the semiconductor package 11E' bears substantial similarity to the semiconductor package 11E shown and described above in relation to Figure 8A, except that the leads 34 in the semiconductor

package 11E' are inverted in the same manner the leads 34 are inverted in the semiconductor package 11A'. The inversion of the leads 34 in the semiconductor package 11E' allows for the electrical connection of the second external lead semiconductor package 58 thereto in the manner shown in Figure 14A.

Figure 14B is a cross-sectional view of a thirtieth exemplary embodiment of the present invention which shows a stacked semiconductor package arrangement similar to that shown in Figure 12A, except that the semiconductor package 11F' shown in Figure 14B includes the above-described interposer 6 as an alternative to the interposer 2 included in the semiconductor package 11A'. In this regard, the semiconductor package 11F' bears substantial similarity to the semiconductor package 11F shown and described above in relation to Figure 8B, except that the leads 34 in the semiconductor package 11F' are inverted in the same manner the leads 34 are inverted in the semiconductor package 11A'. The inversion of the leads 34 in the semiconductor package 11F' allows for the electrical connection of the second external lead semiconductor package 58 thereto in the manner shown in Figure 14B.

This disclosure provides exemplary embodiments of the present invention. The scope of the present invention is not limited by these exemplary embodiments. Numerous variations, whether explicitly provided for by the specification or implied by the specification, such as variations in structure, dimension, type of material and manufacturing process may be implemented by one of skill in the art in view of this disclosure.